Development of Custom FPAA Hardware for Faster Than Real-Time Analysis of Power System Dynamics

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Introduction

• Presentation reviews authors work in field of:
  – Analog emulation of power system dynamics;
  – Via field-programmable analog array (FPAA) technology.
• Specifically, it discusses new emulation tool.
  – Increased modularity and operator density;
  – For larger power systems and smart grids.
• Several innovative aspects:
  – One is use of custom FPAA boards;
  – Developed at Drexel University and The College of New Jersey.
Introduction

• Work places emphasis on:
  – Decreased prototype size;
  – Increased density of computational analog blocks (CAB’s);
  – More effective FPAA interconnection scheme;
  – Batch-mode FPAA configuration.

• New prototype is smaller and faster.
  – Utilizes on-board RAM for auto-configuration.
Why Analog Emulation?

• What is analog emulation, again?
  – Model system;
  – Build analog circuits to emulate dynamics;
  – Initialize and run;
  – Measure solution.

• Today, digital simulation is popular for nonlinear system analysis.
  – More flexible and easier to configure;
  – More precise;
  – Smaller, cheaper, and more less power hungry.
Why Analog Emulation?

• Why bother studying analog emulation? Motivation?
  – Improvement of FPAA technology;
    • FPAA is more flexible, more precise, smaller, etc...
    • Comparable to digital technology, in many ways.
  – Speed;
    • (Faster-than) real-time;
    • Emulation doesn’t use iterative numerical techniques;
    • Computation time is controllable, independent of size and complexity.
• Throughout history, analog computers have been used.
  – They have demonstrated their potential solve transient and nonlinear problems faster than is possible numerically.
Authors’ Previous Work

• Authors created three emulator prototypes.
  – First in 2006, using traditional components.
    • Gens, lines, and loads for 3-bus system.
  – Second in 2010, using commercial FPAA boards.
    • Gens, lines, and loads for 3-bus system.
    • Gens, lines, and loads for 5-bus system.
• All use NI’s DAQ hardware.
Problem Statement

- FPAA may be used to develop analog computing HW.
  - With many positive characteristics associated with digital.
- However, FPAA scalability is still limited.
  - Difficult to interconnect FPAA;
  - Difficult to configure multiple boards at once.
- Commercial FPAA (e.g. Anadigm) are designed for basic problems.
  - Filtering;
  - Analog signal processing.
- They are not designed for more complex implementations.
Problem Statement

- Specific FPAA **scalability issues** include:
  - Low **CAB** density;
    - Unlike modern field programmable gate arrays (FPGA’s) that contain between 500k and 2M logic cells, the Anadigm AN231E04 FPAA houses only four computational analog blocks (CAB’s).
  - Need for manual **interconnection**;
  - Ineffective batch-mode **configuration**;
    - More than **three arrays** cannot be configured in series;
    - Unless digital hardware is used to **boost signal strength**.
  - **Size**.
    - FPAA development board is 25in\(^2\), but **chip is only 1in\(^2\)**.
Proposed Solution

• How do authors address problematic issues on previous slide?
  – Design and fabrication of custom FPAA hardware;
  – Increase FPAA density – 0.16 to 1.06 CAB’s / in²;
  – Modularize design – standardize pin connections.
    • Still requires manual interconnection, unfortunately;
    • However, modularity does make automation easier.
  – Batch-mode configuration via microcontroller;
    • Design may be uploaded to PIC18F4620 from PC;
    • Microcontroller then uploads configuration to all FPAAs.
  – Consolidate auxiliary components – like power supplies.

There are four main design objectives in this work.
Figure #2: Preliminary FPAA-based Analog Power System Emulator Prototype Design

Figure #3: Completed FPAA-Based Analog Power System Emulator Prototype
Prototype Details

- Designed at Drexel University and The College of New Jersey.
- Board contains 17-Anadigm AN231E04 FPAA chips.
  - As well as 1-Microchip PIC18F4620 microcontroller.
- 6.4 by 10 inch, four-layer printed circuit board (PCB).
- 17 differential analog inputs, 18 differential analog outputs
- Contain four-buses and three transmission lines.
  - Second-order swing equation generator model;
  - First-order exponential PQ-bus load model;
- Performs steady-state and transient analyses.
  - Examples include load flow and generator fault studies.
Component Models Used

general form: \( \frac{d^2 \theta_2}{dt^2} = \frac{1}{(\tau_{2\text{ang}})^2} \left( \sum P_k - P_{i\text{ inj}} \right) \)

\[
\begin{align*}
\frac{d^2 \theta_2}{dt^2} &= \frac{1}{(\tau_{2\text{ang}})^2} \left[ P_{21} \left( V_{2\text{ re}} I_{21\text{ re}} + V_{2\text{ im}} I_{21\text{ im}} \right) + P_{23} \left( V_{2\text{ re}} I_{23\text{ re}} + V_{2\text{ im}} I_{23\text{ im}} \right) + \ldots \right] \\
& \quad \ldots + \left( V_{2\text{ re}} I_{\text{ext 2 re}} + V_{2\text{ im}} I_{\text{ext 2 im}} \right) - P_{2\text{ inj}}
\end{align*}
\]

second-order
swing equation
for PV generator

\[
\begin{align*}
\frac{d}{dt} \left| \bar{V}_3 \right| &= \frac{1}{\tau_{3\text{ mag}}} \left[ Q_{34} \left( V_{3\text{ im}} I_{34\text{ re}} - V_{3\text{ re}} I_{34\text{ im}} \right) + Q_{32} \left( V_{3\text{ im}} I_{32\text{ re}} - V_{3\text{ re}} I_{32\text{ im}} \right) + \ldots \right] \\
& \quad \ldots + \left( V_{3\text{ im}} I_{\text{ext 3 re}} - V_{3\text{ re}} I_{\text{ext 3 im}} \right) - Q_{3\text{ inj}}
\end{align*}
\]

first-order
exponential
recovery model
for PQ load

\[
\begin{align*}
\frac{d \theta_3}{dt} &= \frac{1}{\tau_{3\text{ ang}}} \left[ P_{34} \left( V_{3\text{ re}} I_{34\text{ re}} + V_{3\text{ im}} I_{34\text{ im}} \right) + P_{32} \left( V_{3\text{ re}} I_{32\text{ re}} + V_{3\text{ im}} I_{32\text{ im}} \right) + \ldots \right] \\
& \quad \ldots + \left( V_{3\text{ re}} I_{\text{ext 3 re}} + V_{3\text{ im}} I_{\text{ext 3 im}} \right) - P_{3\text{ inj}}
\end{align*}
\]
Figure #4: Emulated Three-Bus Power System Composed of Infinite Bus, P|V| Generator, and PQ Load, Highlighting Data Flow

**Infinite Bus is represented by constant voltage sources.**

**Buses #1 and #4 may be shorted together to create traditional three-bus system.**

**Current measurements may be provided to adjacent modules.**

**Current measurements may be acquired from adjacent modules.**

**The initial condition \((V_2^0, V_3^0)\) is applied at buses #2 and #3 until IC release.**

**Generator emulation circuit utilizes \(I_{12}, I_{23},\) and \(I_{\text{ext}2}\) as input and updates \(V_2\) via swing equation.**

**Load emulation circuit utilizes \(I_{43}, I_{23},\) and \(I_{\text{ext}3}\) as input and updates \(V_3\) via exp. recovery model.**

**X-Line emulation circuit utilizes \(V_i\) and \(V_k\) as input and generates \(I_{ik}\).**

**Current measurements may be provided to adjacent modules.**
Modularity

- Each consists of four buses.
- Buses #2 and #3 contain integrators that “solve.”
- Buses #1 and #4 facilitate interconnection.
  - Pass in / out current flow.
- What about infinite bus?
  - Connect #1 and #4 to constant voltage source.

Figure #5: Example of Nine-Bus Power Emulated with Four of the Authors’ FPAA Modules (Manual Placement of Jumper Wires Shown with Dashed Line)
Figure #6: Highlight of Adjacent Module Interconnection
### Size

Table #1: Emulator vs. Power System Size for Third Prototype Shown in Figure 4. It assumes that PCB boards are stacked vertically with 0.5 inch spacing and maximum of 100 boards per stack.

<table>
<thead>
<tr>
<th># buses (modules)</th>
<th># boards</th>
<th># FPAAs</th>
<th>prototype dimensions (and volume)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1</td>
<td>17</td>
<td>6.4in, 10in, 0.5in (32in³)</td>
</tr>
<tr>
<td>21</td>
<td>10</td>
<td>170</td>
<td>6.4in, 10in, 5in (320in³)</td>
</tr>
<tr>
<td>201</td>
<td>100</td>
<td>1700</td>
<td>6.4in, 10in, 4.2ft (1.85ft³)</td>
</tr>
<tr>
<td>2001</td>
<td>1000</td>
<td>17000</td>
<td>2.7ft, 1.6ft, 4.2ft (18.5ft³)</td>
</tr>
</tbody>
</table>
Testing and Validation

- To evaluate the new prototype, a **five-bus test system** was used.
- Two FPAA emulator modules were interconnected.

![Five-Bus Test System Diagram](image-url)

Figure #7: Five-Bus Test System
Figure #8: Five-Bus Test System in Hardware
Testing and Validation

• Authors used hardware to perform critical clearing time study.
  – 3-phase, line-to-ground fault
• Repetitive transient analyses performed, with increasing \( t_{fault} \).
  – Stopped once system fails to recover / stabilize.
• Following values were observed:
  – Steady-state \( V \) and \( \theta \) solutions, no fault;
  – Settling time \( (t_{settle}) \), no fault;
  – Critical clearing time \( (t_{cc}) \).
• National Instruments DAQ hardware used to observe system.
Figure 9-12: Solution Error (as Compared to Simulation in Mathworks' Matlab) for (Top-Left) Steady-State Voltage Magnitude, (Top-Right) Steady-State Voltage Angle, (Bottom-Left) Settling Time, and (Bottom-Right) Critical Clearing Time.

- Steady-State Voltage Magnitude Solution, No Fault
- Steady-State Voltage Angle Solution, No Fault
- Settling-Time, No Fault
- Critical Clearing Time
Sources of Error

• Need for opamp chopping (chopping-stabilization)
  – Need to activate multipliers’ opamp chopping option.
  – Needed to improve response to rapidly-changing signals.
  – Increases FPAA resources by 20%.

• Discrepancies between hardware and simulation
  – Anadigm Designer 2 may not generate accurate results.
  
This is very important. Although it is not sufficiently highlighted in hardware’s documentation.

• Common-mode input
  – Optimally, common-mode inputs equal approximately 1.5V.
Sources of Error

- Loading and need for sample-and-hold.
  - Many CABs have limited loading capability;
  - Sample-and-hold needed to supply output to multiple CABs.
    - Used as buffer.
  - Otherwise, device may supply abnormally-low voltage.
Conclusion

• Study application of analog emulation to power systems.
  – Innovative because it utilizes FPAA technology.
• Previous works illustrate strengths/weaknesses of emulation.
  – Both traditional analog and FPAA.
• This work addresses lack of FPAA hardware scalability.
• Researchers developed third analog emulator at Drexel.
• Test results are sub-optimal, but promising.
  – May be attributed to number of attempts to address problems on-the-fly, without total redesign.
• Future prototypes will focus on eliminating “sources of error.”
Questions?